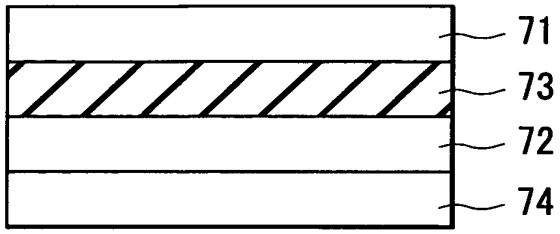


FIG. 1

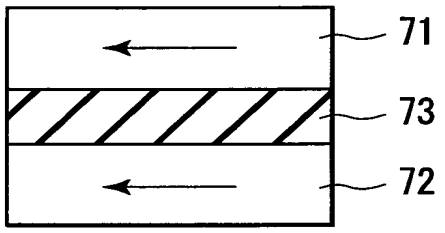


FIG. 2A

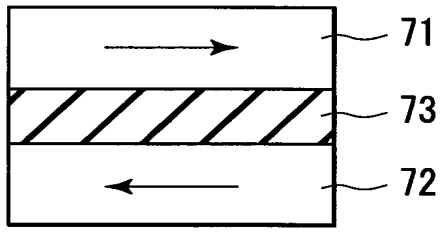


FIG. 2B

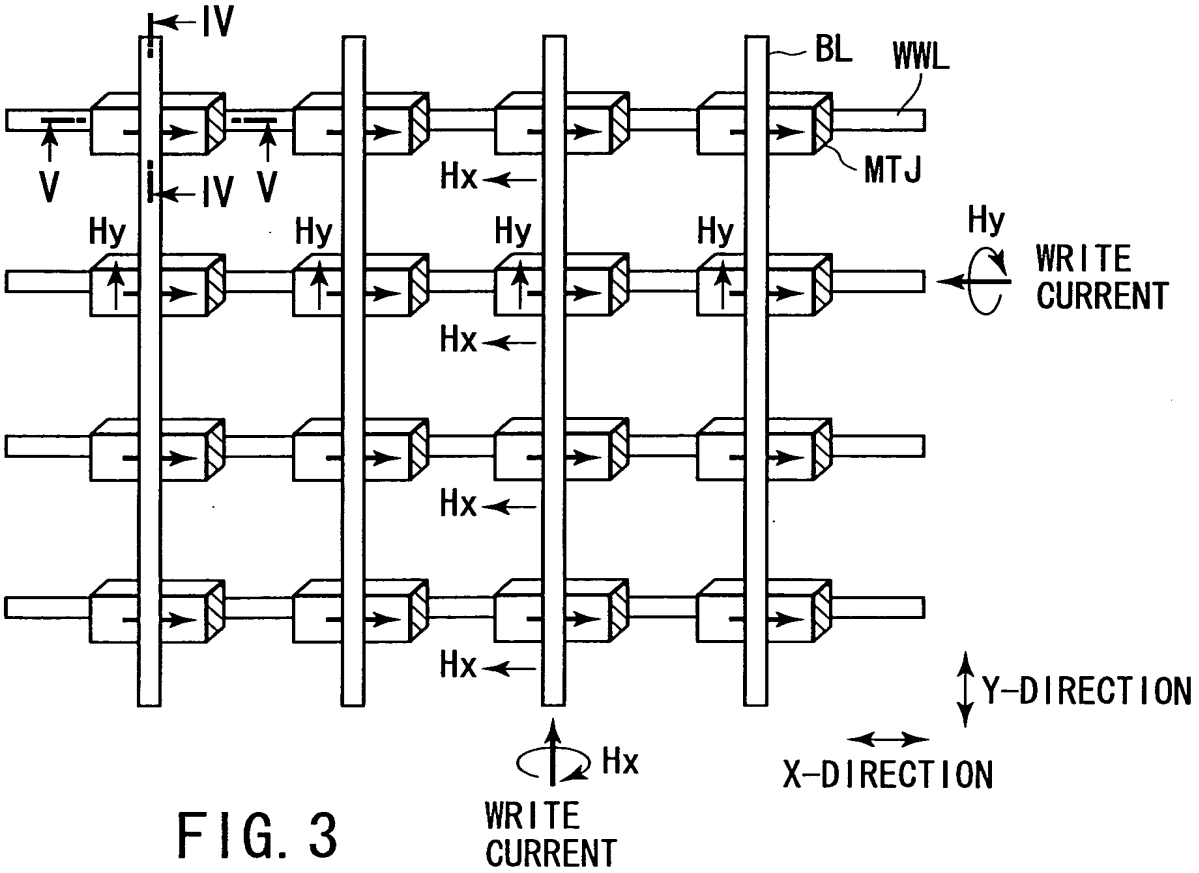


FIG. 3

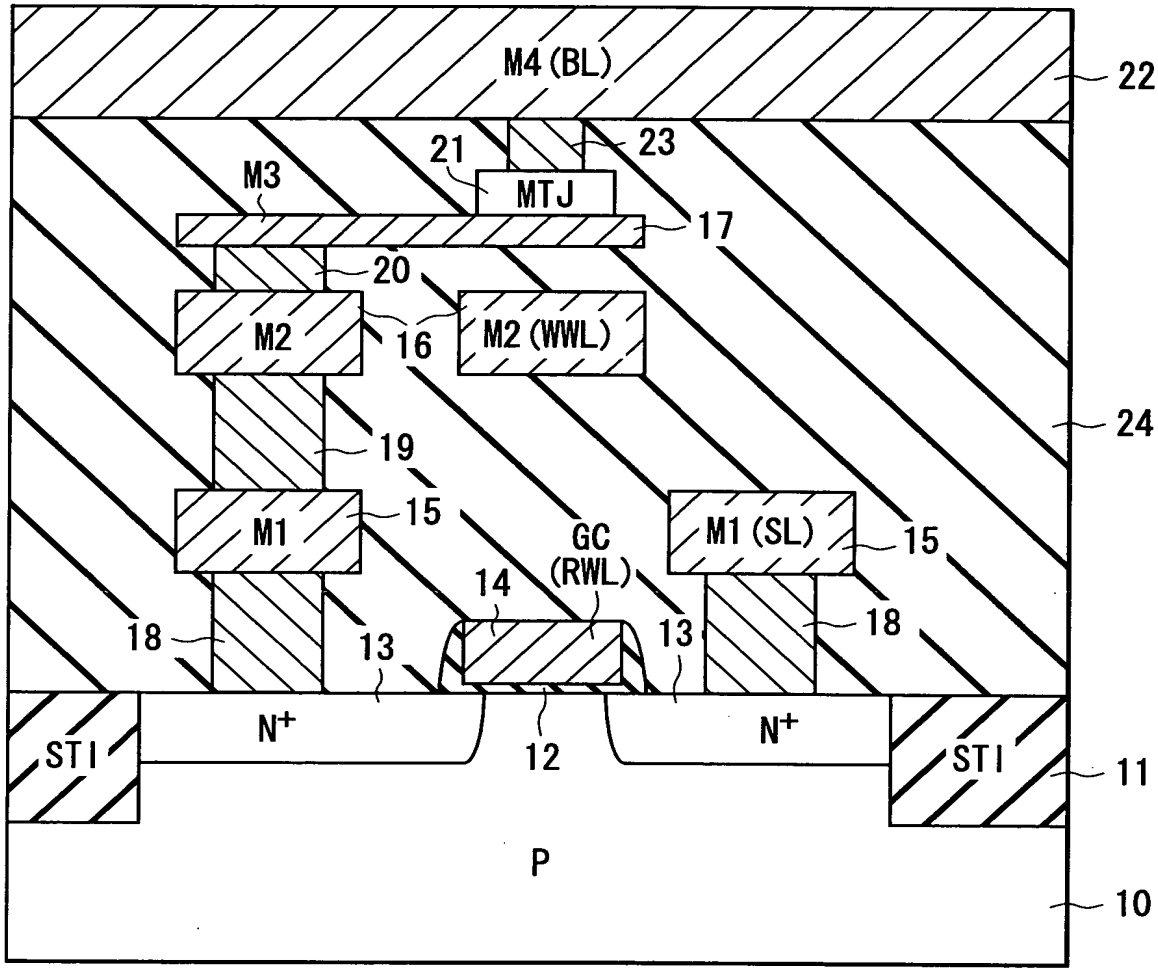

M4 (BL)
22
21
23
M3
MTJ
17
20
M2
16
M2 (WWL)
24
19
M1
15
GC
(RWL)
M1 (SL)
15
14
18
13
13
18
N+
N+
STI
12
STI
11
P
10

FIG. 4

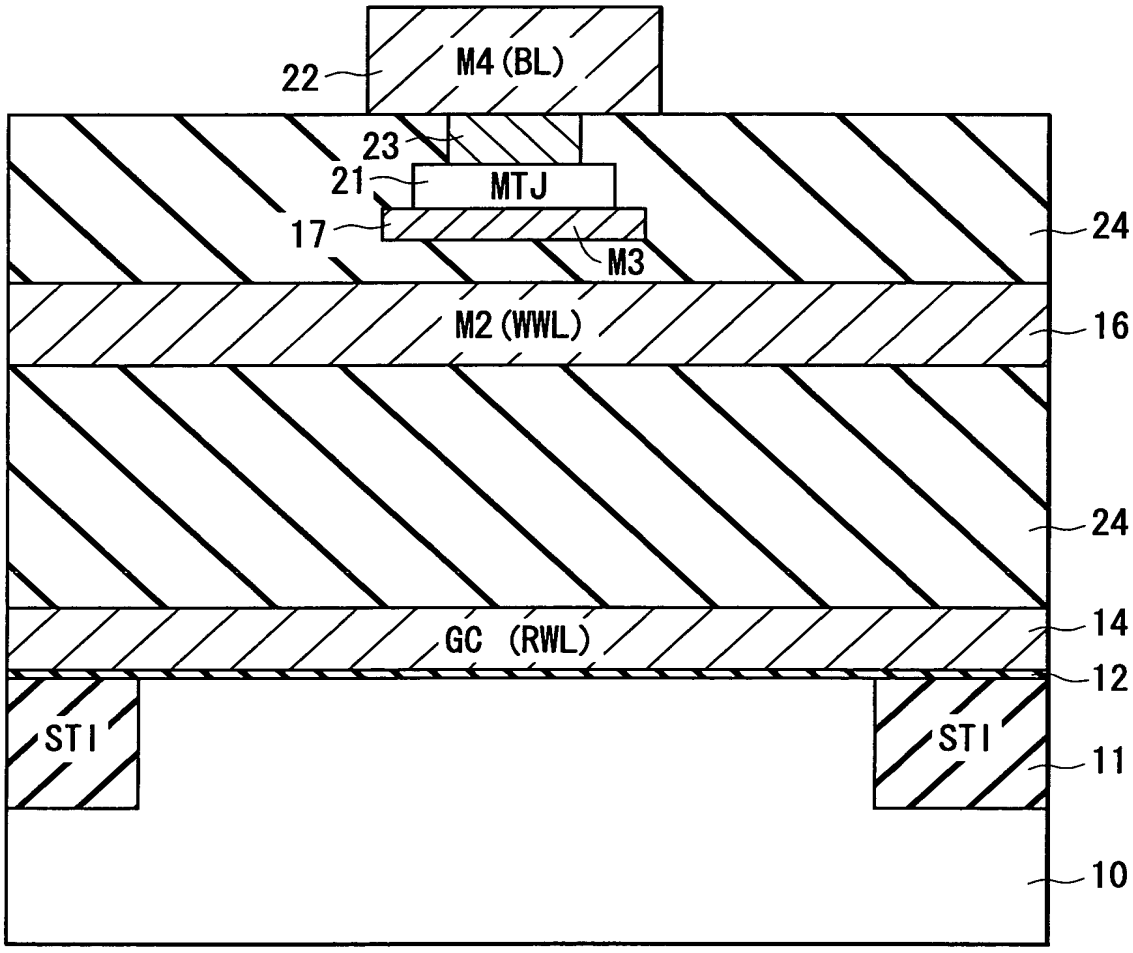
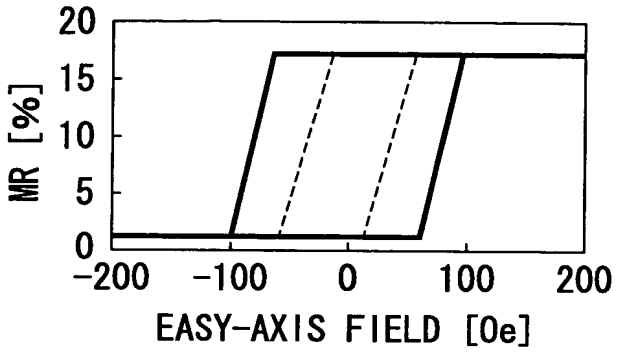


FIG. 5

FIG. 6



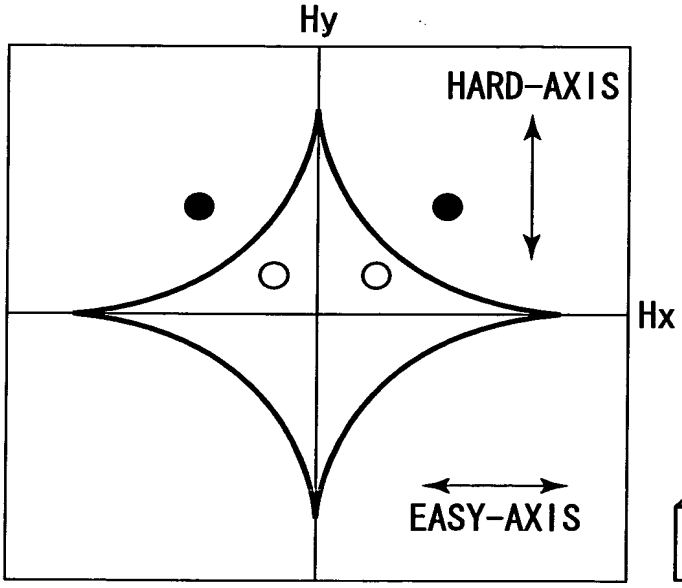


FIG. 7

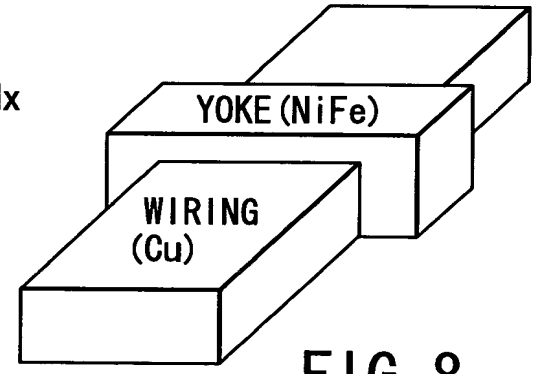


FIG. 8

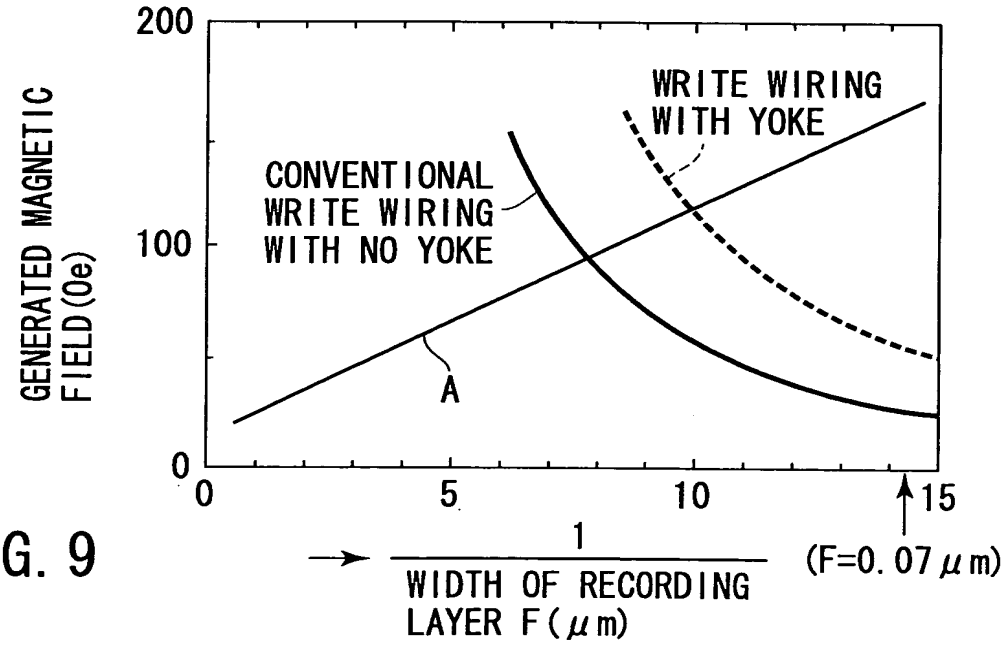


FIG. 9

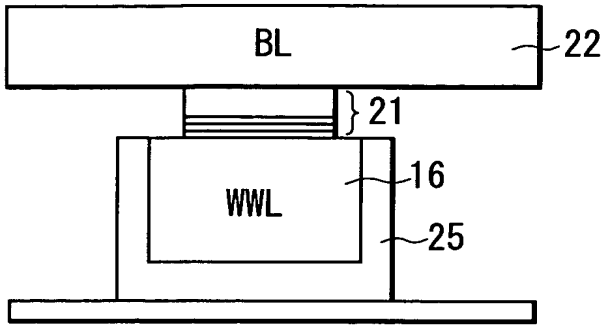


FIG. 10

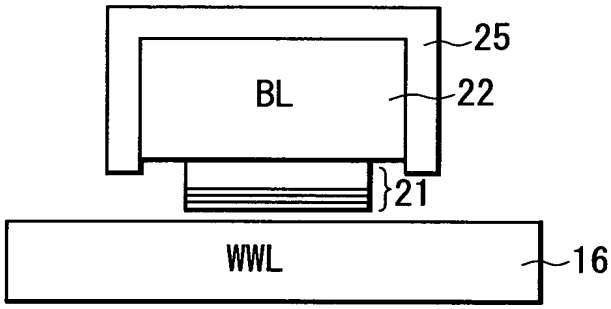


FIG. 11

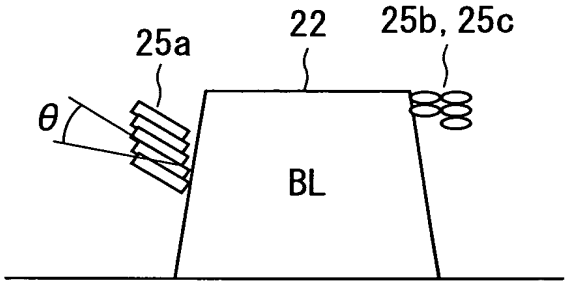


FIG. 12

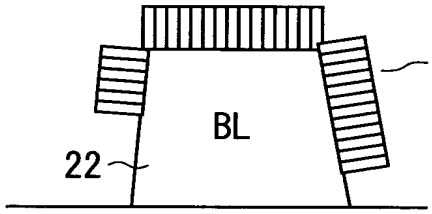


FIG. 13A

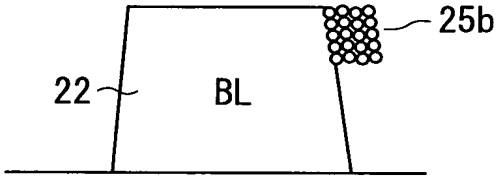


FIG. 13B

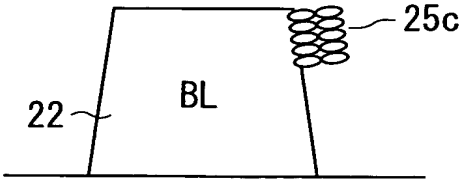


FIG. 13C

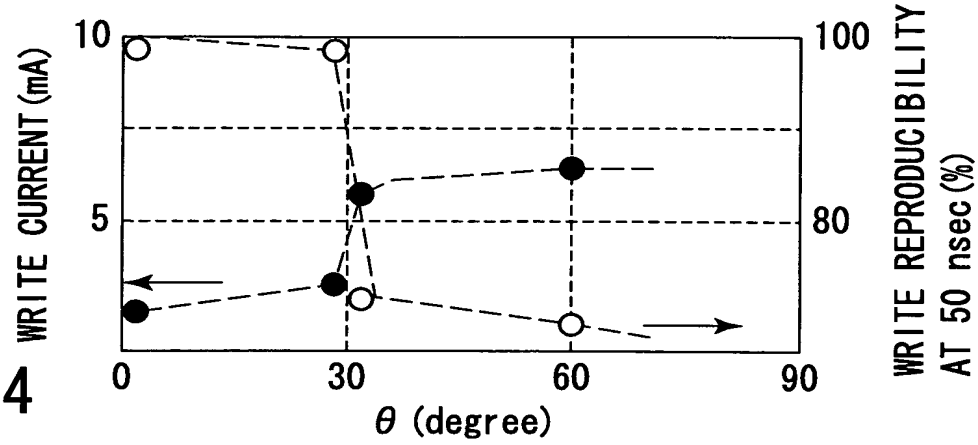


FIG. 14

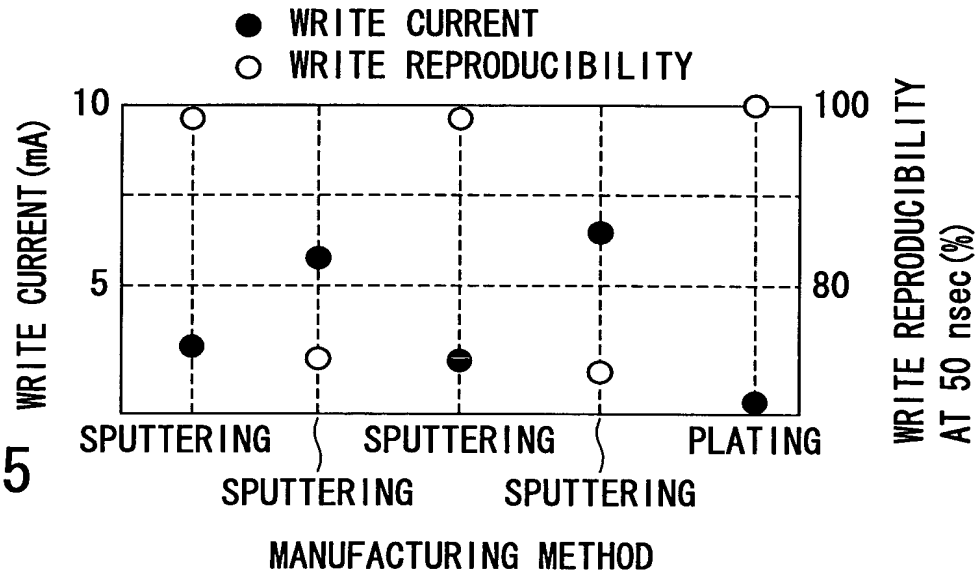


FIG. 15

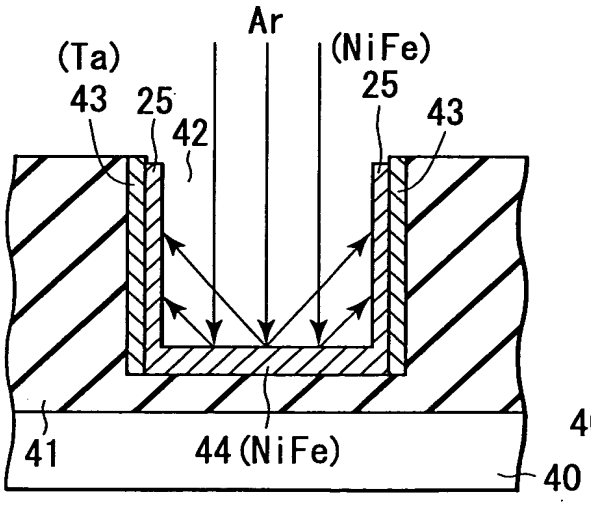


FIG. 16

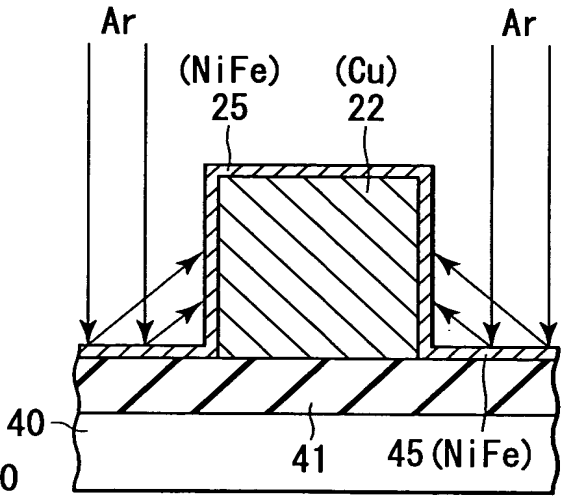


FIG. 17

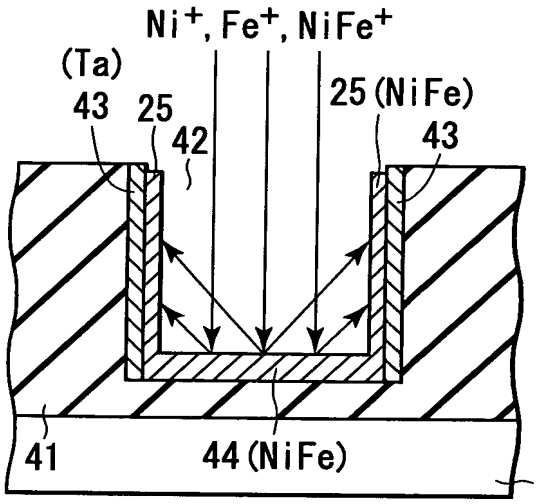


FIG. 18

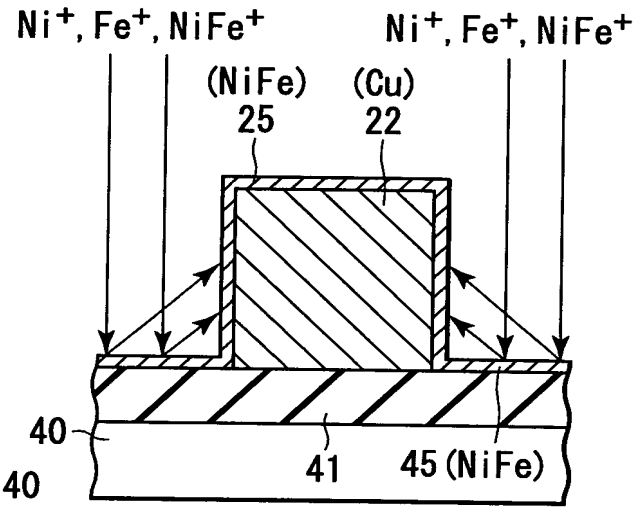


FIG. 19

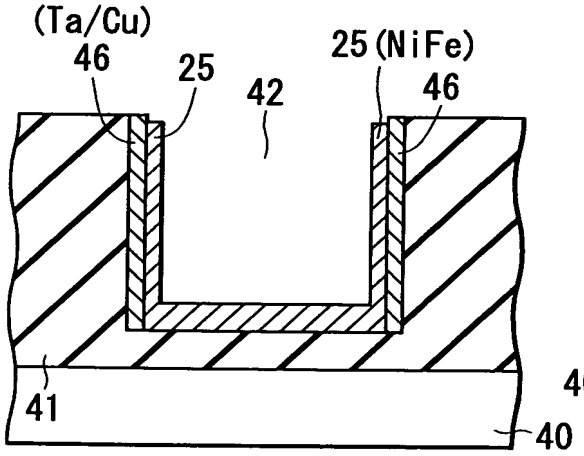


FIG. 20

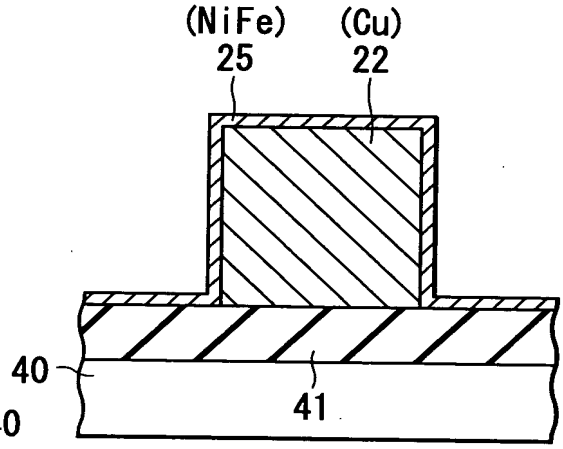


FIG. 21

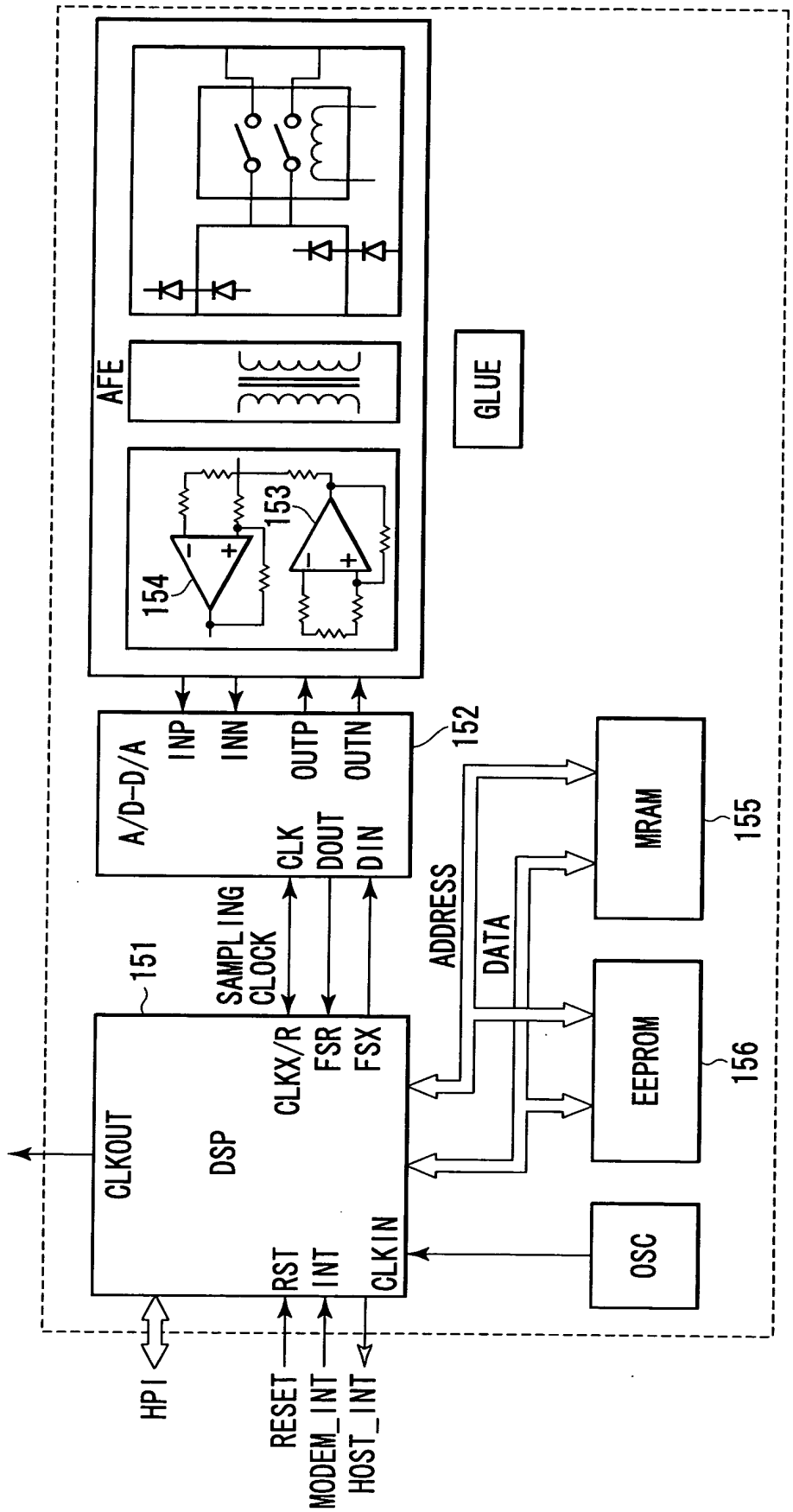

AFE
GLUE
153
154
A/D-D/A
INP
INN
OUTP
OUTN
152
CLK
DOUT
DIN
SAMPLING CLOCK
151
ADDRESS
DATA
MRAM
155
EEPROM
156
CLKOUT
DSP
CLKX/R
FSR
FSX
RST
INT
CLKIN
OSC
HPI
RESET
MODEM_INT
HOST_INT

FIG. 22

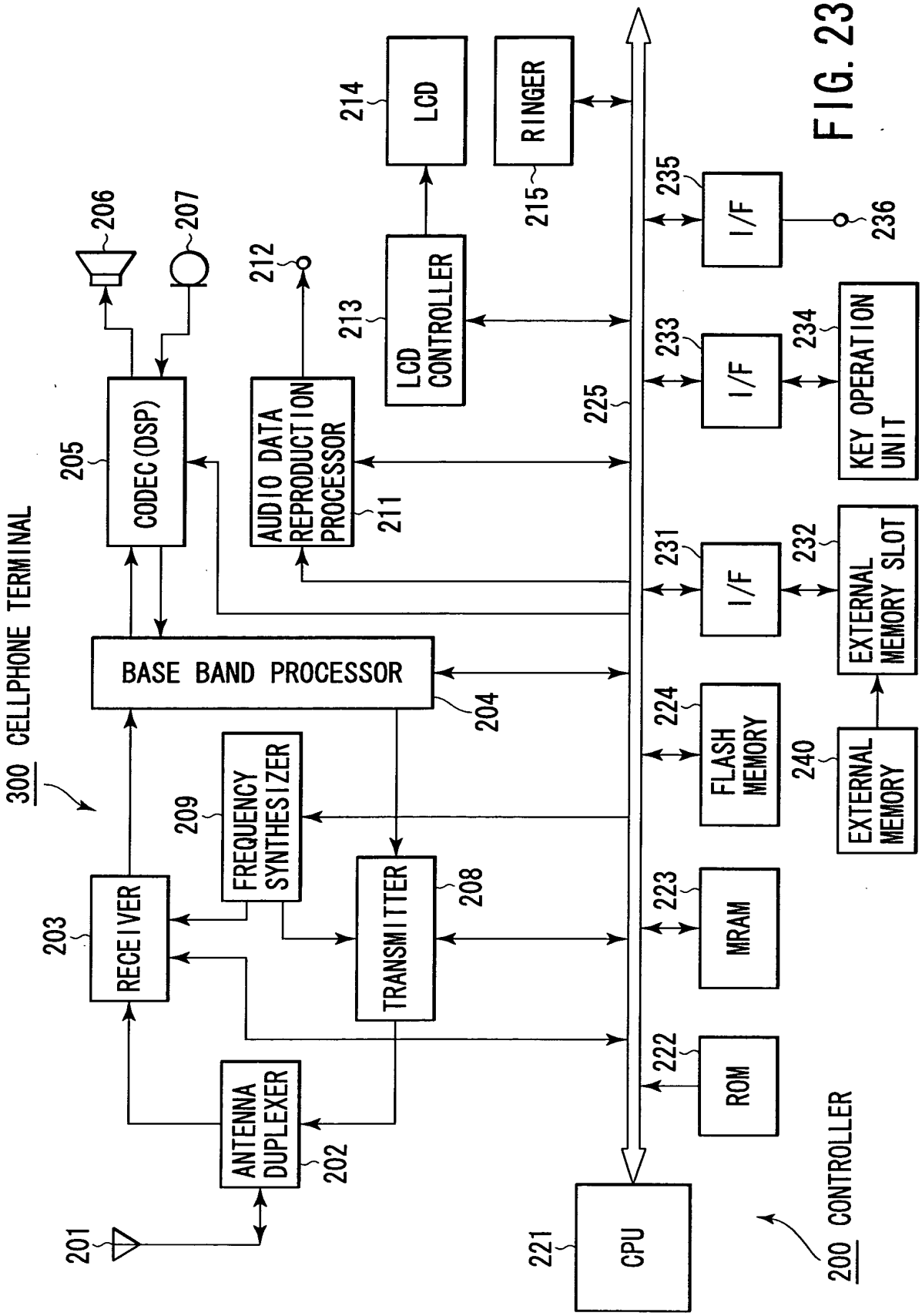

300 CELLPHONE TERMINAL
200 CONTROLLER
201
202
ANTENNA DUPLEXER
203
RECEIVER
204
BASE BAND PROCESSOR
205
CODEC (DSP)
206
207
208
TRANSMITTER
209
FREQUENCY SYNTHESIZER
211
AUDIO DATA REPRODUCTION PROCESSOR
212
213
LCD CONTROLLER
214
LCD
215
RINGER
221
CPU
222
ROM
223
MRAM
224
FLASH MEMORY
225
231
I/F
232
EXTERNAL MEMORY SLOT
233
I/F
234
KEY OPERATION UNIT
235
I/F
236
240
EXTERNAL MEMORY

FIG. 23

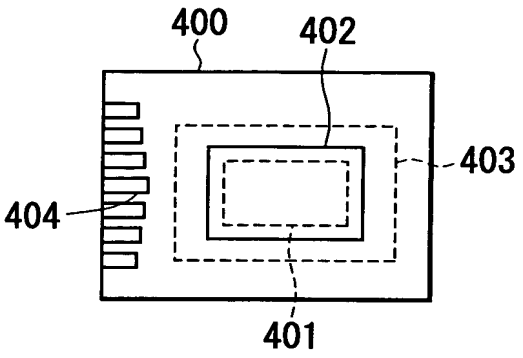


FIG. 24

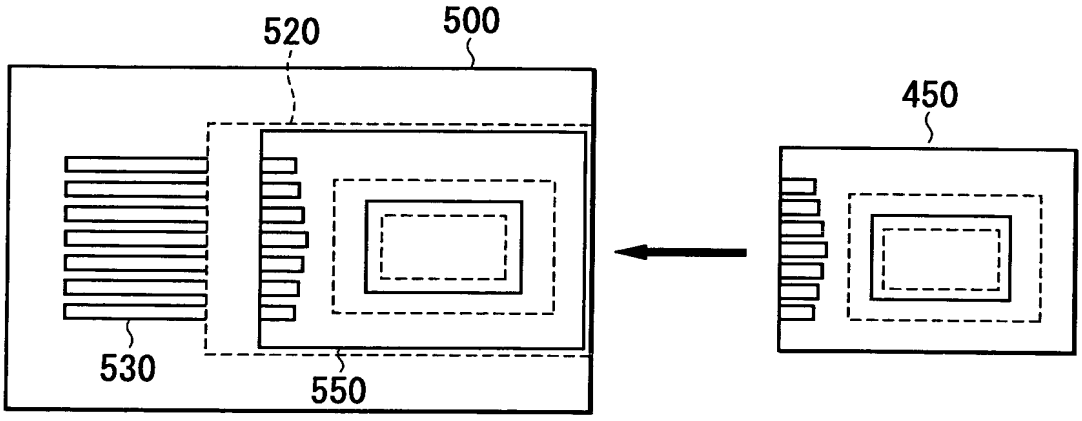
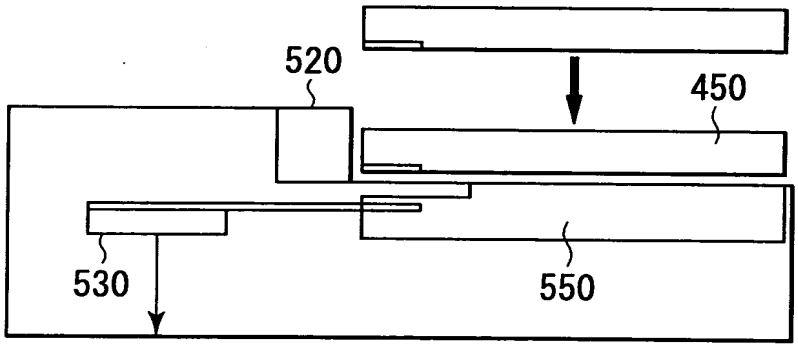


FIG. 25



TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 27

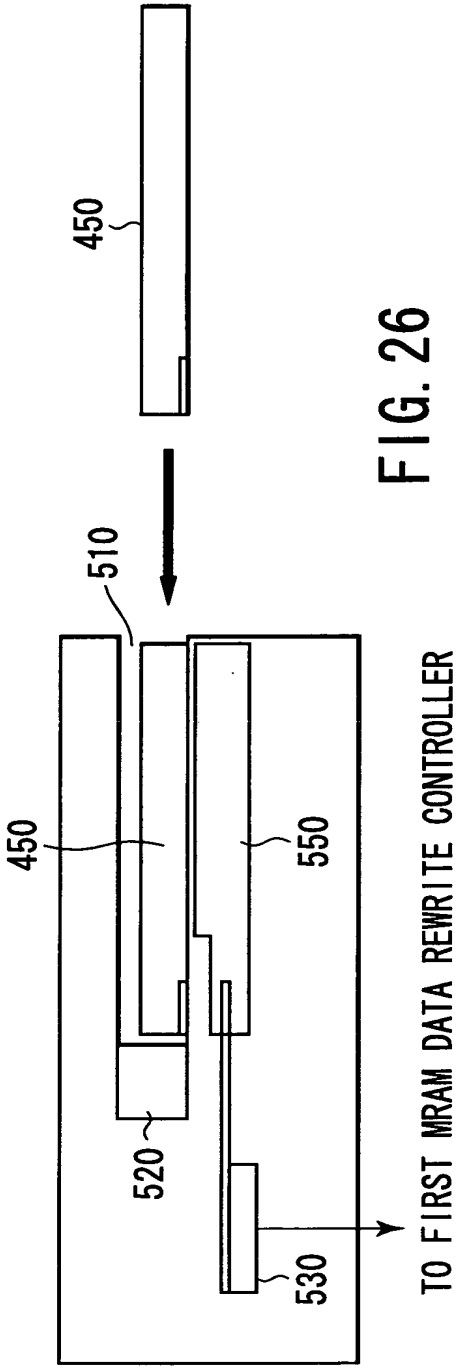

450
510
450
550
520
530
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 26

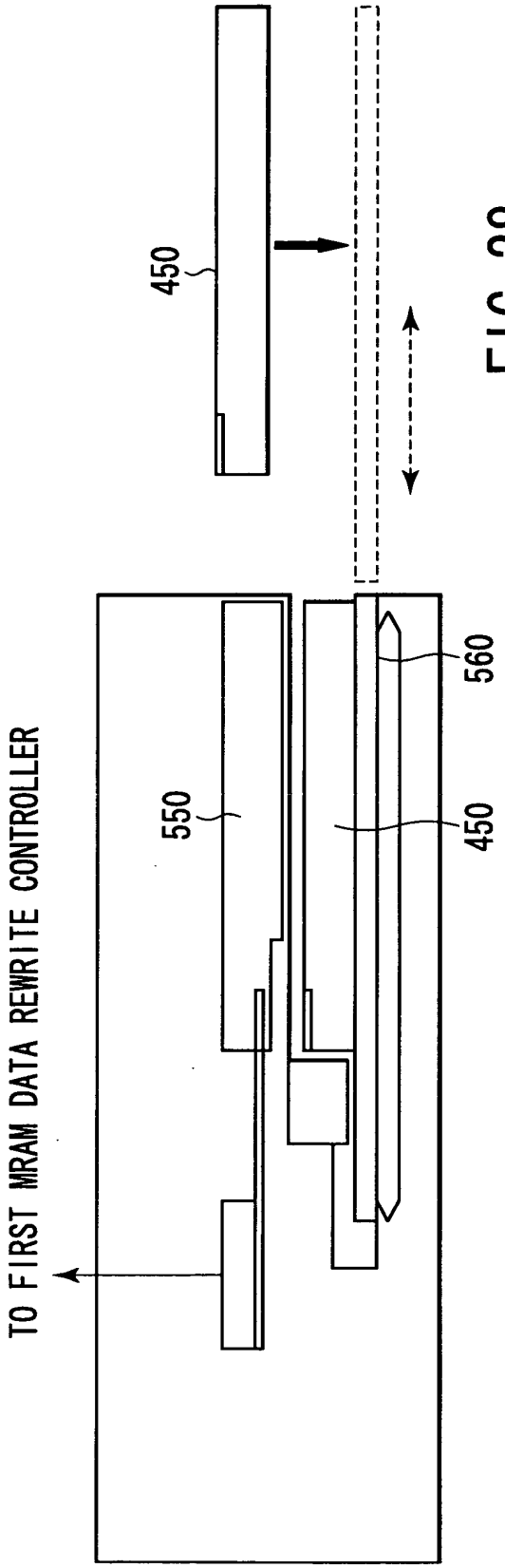

450
560
550
450
TO FIRST MRAM DATA REWRITE CONTROLLER

FIG. 28